## REMARKS

All of the pending claims in this application have been rejected by the Office Action dated September 18, 2003. In response to the Office Action, applicants submit the following remarks and respectfully request reconsideration of the application.

**Rejection of claims 1- 8 under Section 103(a) should be withdrawn**

Claims 1- 8 were rejected by the Office Action under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 4,705, 967 issued to Vasile (hereinafter "Vasile") in view of U.S. Patent No. 5,333,105 issued to Fortune (hereinafter "Fortune"). Of the allegedly unpatentable pending claims, claim 1 and claim 7 are independent with the remaining pending claims being dependent upon them.

Applicants thank the Examiner for withdrawing the prior rejection of claims 1-8 in view of the previously arguments presented. The Office Action concedes that the Applicants' prior response filed on July 10, 2003 was persuasive. However, the Office Action has rejected claims 1-8 based on a combination of the previously relied upon reference Vasile with the new Fortune reference.

The Fortune reference discloses a circuit for protection against too fast a rate of change of a voltage of interest by using a high pass filter to detect transients to trigger a shunt. Therefore, Fortune discloses protecting electrical devices from transient changes in supply voltages, e.g., in an automobile.

Vasile discloses a circuit for performing multifunctional operation comprising a floating FET having symmetrical source and drain characteristics. Specifically, Vasile discloses that the source and drain of the floating FET are connected to a center-tapped balun, which may receive an unbalanced input and present it as a balanced input to the floating FET.

An additional input may be provided at the gate of the floating FET, which is also biased to avoid pinch-off conditions. In other words, the FET disclosed in Vasile must be normally-on to function.

Vasile does not disclose a method and apparatus for a circuit against over-voltage as is alleged by the Office Action. Instead, it expressly notes that the amplitudes of the input signals are understood to be small. See, e.g. col. 7, lines 25-27. This feature of Vasile argues against interpreting it as a protection circuit in the absence of more detailed reasons to support the rejection of the invention of claim 1, which is directed to the undesiarable effects of a transient overvoltage.

This feature of Vasile is not surprising since the circuit depicted in Figure 5 actually integrates the product of the input signals (received at the gate and the balun) as shown in the figure itself (and its description) to generate a cumulative output. In light of this stated aim, it is not surprising that unlike the claimed invention, where the gate of the bidirectional transistor is biased to **ensure** that the transistor is normally off, Vasile biases the gate to **avoid** having the transistor normally off by avoiding pinch-off conditions. See, e.g., column 7, lines 20-25.

In sharp contrast to Vasile, the claimed invention requires the transistor to be "normally-off." Fortune does not cure the requirement (of Vasile) that the FET must be normally-on. Therefore, applicants respectfully request that either the rejection of claims 1-8 be withdrawn or the combination of Vasile and Fortune be explained in sufficient detail to clarify how the their divergent teachings and objectives are to be reconciled without essentially relying on impermissible hindsight.

Applicants are unclear as to the Office Action's motivation for discarding the integrative function of Vasile, which is actually directed to perform multifunctional operations rather than the alleged "circuit against over-voltage." The integrative function would be defeated if the transistor is normally-off in the combination of Vasile and Fortune. Therefore, it is respectfully requested that the reasons and details of the combination of Fortune with Vasile be sufficiently clearly described to provide the reasons for treating their apparently conflicting goals and designs as being compatible. This would also allow a more detailed response to be presented by the applicants.

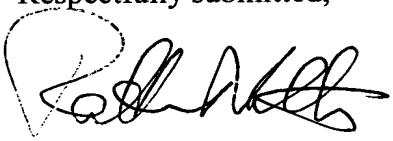
In addition, shunting of all high frequency signals by a high-pass filter, as disclosed by Fortune, is undesirable for proper processing of high frequency signals. Therefore, as a preliminary matter, Fortune will interfere with the processing of such signals since Fortune is compatible with little more than protection against rapid changes in a DC supply voltage. In other words, there is no motivation within the record, other than pure hindsight (which is impermissible) to combine the apparently incompatible Vasile and Fortune references. Further, even if they are so combined, they fail to meet all of the limitations of the claimed invention or to enable the invention.

## CONCLUSION

In light of the above, it is respectfully submitted that the present application is in condition for allowance. No new matter has been introduced by way of this response. Should the Examiner have any questions or comments concerning this submission, or any aspect of the application, the Examiner is respectfully invited to call the undersigned at the phone number listed below.

No fee is believed due at this time. Should any fees be required, please charge such fees to Pennie & Edmonds LLP Account No. 16-1150.

Respectfully submitted,



Dated: December 1, 2003

Rattan Nath (Reg. No. 43,827)
for
Barry D. Rein (Reg. No. 22,411)

**PENNIE & EDMONDS LLP**
1155 Avenue of the Americas
New York, New York 10036-2711
(212) 790-9090